UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,125	08/01/2003	Yiqun Lin	125.084US01	3083

7590 10/11/2006

Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339

EXAMINER	
BOWERS, BRANDON	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,125	LIN ET AL.	
	Examiner	Art Unit	
	Brandon W. Bowers	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-5, 7-14, 32, 37 and 50 have been amended. Claims 1-50 are pending in this application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Yin, US Patent No. 6,298,469.

In reference to claim In reference to claim 1, Yin teaches translating select device parameters in a first schematic database associated with a first process (Figures 1 and 3, 115, 115, 118, and 120) to device parameters in a second schematic database associated with a second process (Figure 3, 303, 308), and displaying a design based on the device parameters in the second database (Column lines 19-60).

In reference to claim 2, Yin teaches translating select device parameters in a first layout database associated with a first process (Figures 1 and 3, 115, 115, 118, and 120) to device parameters in a second layout database associated with a second

process (Figure 3, 303, 308), and displaying a design based on the device parameters in the second database (Column lines 19-60).

In reference to claims 3-5 and 8-10, Yin teaches converting cell placements and interconnectivity wires from one coordinate system to another and in so doing, a completely new database (physical, place & route and netlist) of the integrated circuit are created (generated) for new manufacturing process (column 4, lines 43 – 67).

In reference to claims 6-7 and 11-13, Yin teaches wherein the methodology is performed in a graphical interface environment with the ability to display the steps being performed (Column lines 19-60).

In reference to claim 14, Yin teaches setting translation options including resistances, capacitances or sizing options (Column 3, lines 23-42), reading original schematic and layout informations (Figures 1 and 3, 115, 116, 118, and 120), translating the schematic and layout informations (Figure 3, 303, 308) and outputting parameters of the translated schematic and layout informations (column 5, lines 4 –24).

In reference to claims 15-25, Yin teaches converting cell placements and interconnectivity wires from one coordinate system to another and in so doing, a completely new database (physical, place & route and netlist) of the integrated circuit are created (generated) for new manufacturing process (column 4, lines 43 – 67).

In reference to claims 26-27, Yin teaches creating and reading a configuration file wherein the configuration file comprises at least one of the functions in the group of functions comprising, mapping devices, mapping terminals, mapping mask layers, mapping parameters, inserting original device parameters, creating polarity and rotation,

defining resistor and capacitor options, defining interconnect options and defining functions to be triggered after translation (column 4, lines 43 – 67).

In reference to claims 29-36 Yin teaches wherein the methodology is performed in a graphical interface environment with the ability to display the steps being performed (Column lines 19-60).

In reference to claims 37-50 drawn to a computer readable medium containing instruction for performing the methods rejected in claims 14-36 above, the same rejection applies.

Response to Arguments

Applicant's arguments, see response, filed 19 July 2006, with respect to the Hall rejections have been fully considered and are persuasive. The rejection of 1-13 using the Hall reference have been withdrawn.

Applicant's arguments regarding the Yin rejection have been fully considered but they are not persuasive. In response to claim 1, applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a very narrow interpretation of what a schematic database is and how it functions) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Yin describes "The Netlist Database 116 includes the

connectivity information providing a full logic description of the integrated circuit". In a reasonably broad interpretation, the Netlist Databases of Yin are schematic databases. With regards to claims 14 and 37, applicant argues that Yin does not teach "wherein setting translation options further comprises at least one of an option from a group of options comprising, setting select resistances to remain unchanged, setting select capacitances to remain unchanged and setting select geometries to remain unchanged." However Yin anticipates this by stating "Typically the approach would be to linearly scale down or "shrink" the different devices that are part of the design. However, this is oftentimes not adequate or practical because (1) not all the layout design rules (constraints), i.e. "contact" size and "metal overlapping contact amount" do not change by the same proportion, and (2) not all the devices (therefore circuit parameters) change at the same rate. That is, a resistor utilized in the integrated circuit may change at one rate from one to another process where a transistor in the same circuit may change at another when manufacturing is transferring the manufacturing from one process to another. In addition, through this conventional process it is not possible to obtain an accurate simulation model when moving from one process to another. Applicant, through the present invention, has provided a method for being able to move from process to process and still have accurate information about the device. (Column 3, lines 22-33).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W. Bowers whose telephone number is (571)272-1888. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571)272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BWB

JACK CHIANG
SUPERVISORY PATENT EXAMINER